FIG.1

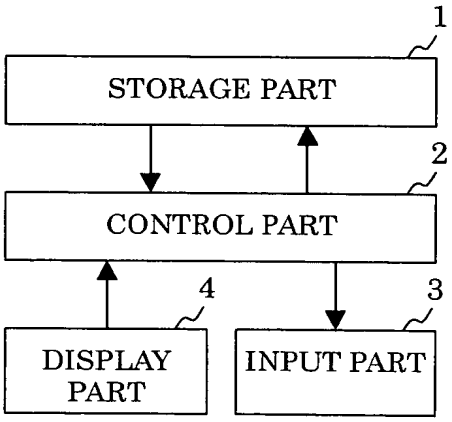

1
STORAGE PART
2
CONTROL PART
4
3
DISPLAY PART
INPUT PART

FIG.2

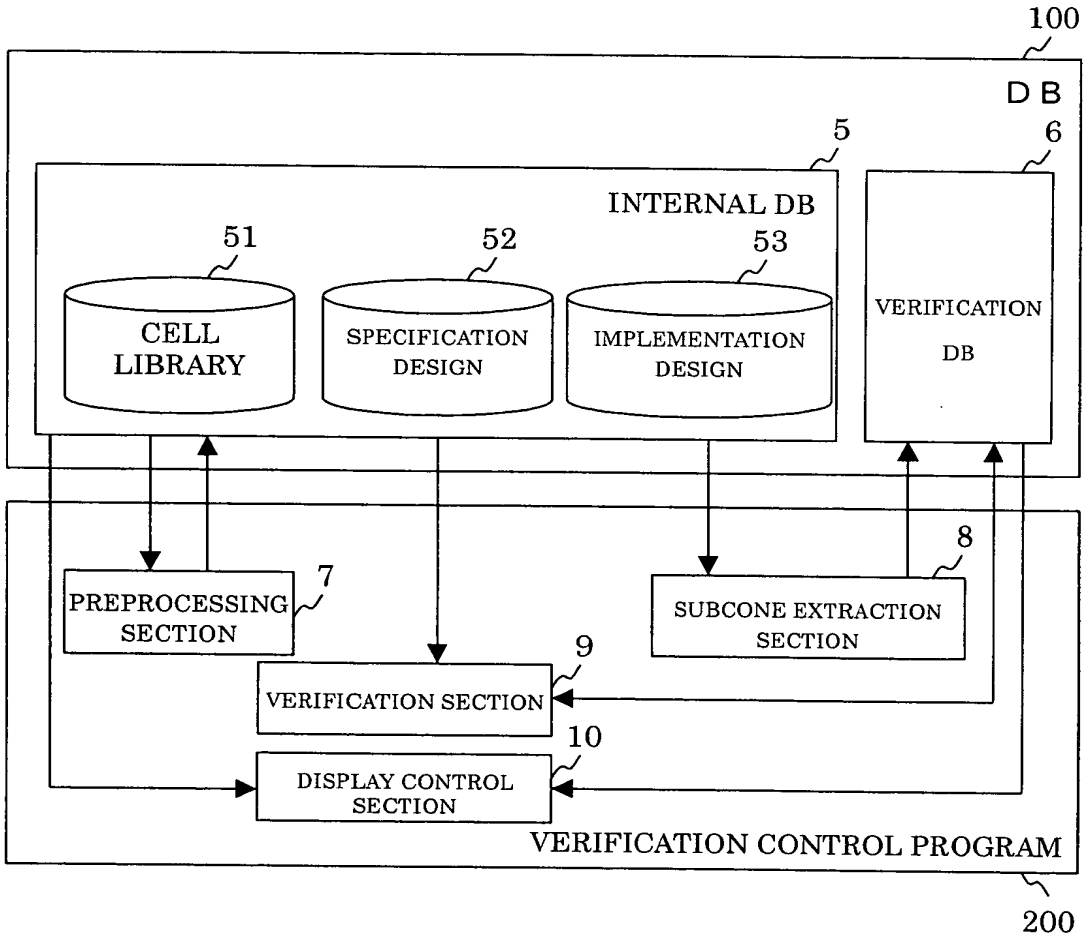

100
DB
5
6
INTERNAL DB
51
52
53
CELL LIBRARY
SPECIFICATION DESIGN
IMPLEMENTATION DESIGN
VERIFICATION DB
8
7
PREPROCESSING SECTION
SUBCONE EXTRACTION SECTION
9
VERIFICATION SECTION
10
DISPLAY CONTROL SECTION
VERIFICATION CONTROL PROGRAM
200

FIG. 3

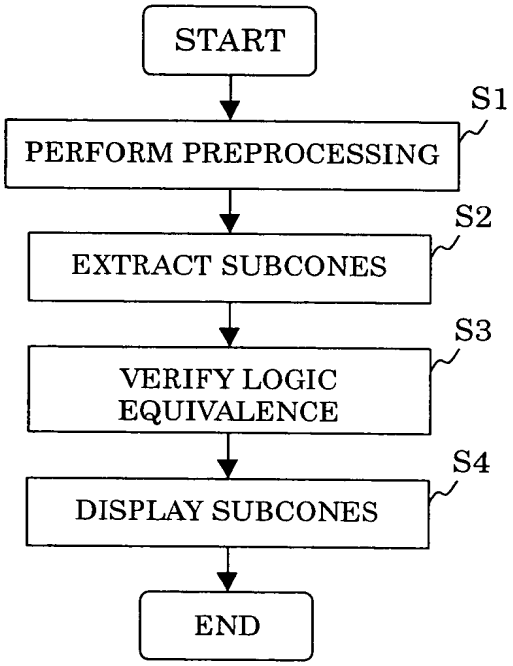


FIG. 4A

FIG. 4B

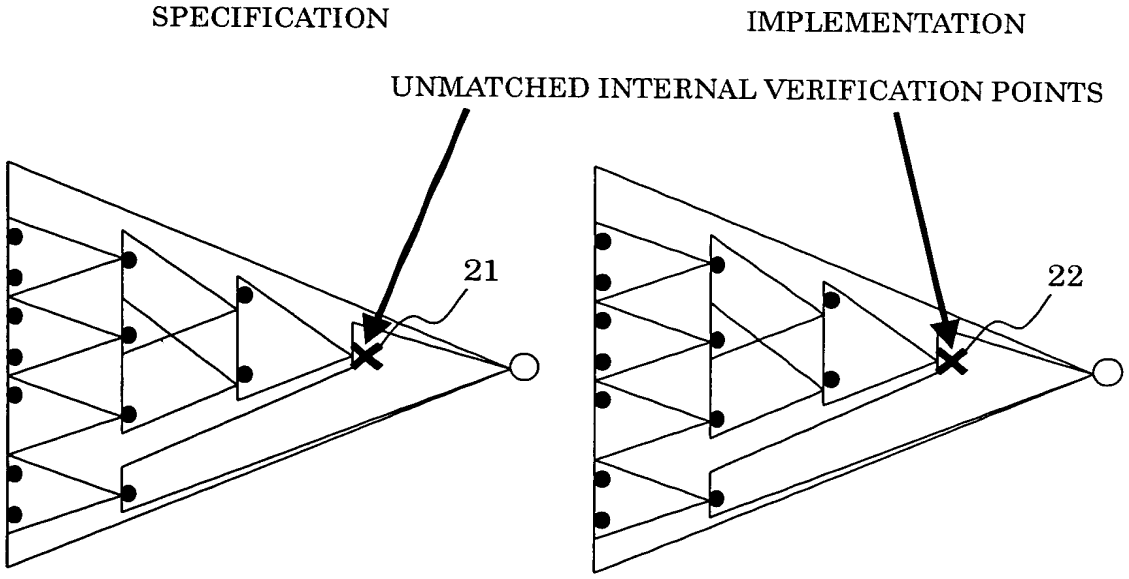


FIG. 5

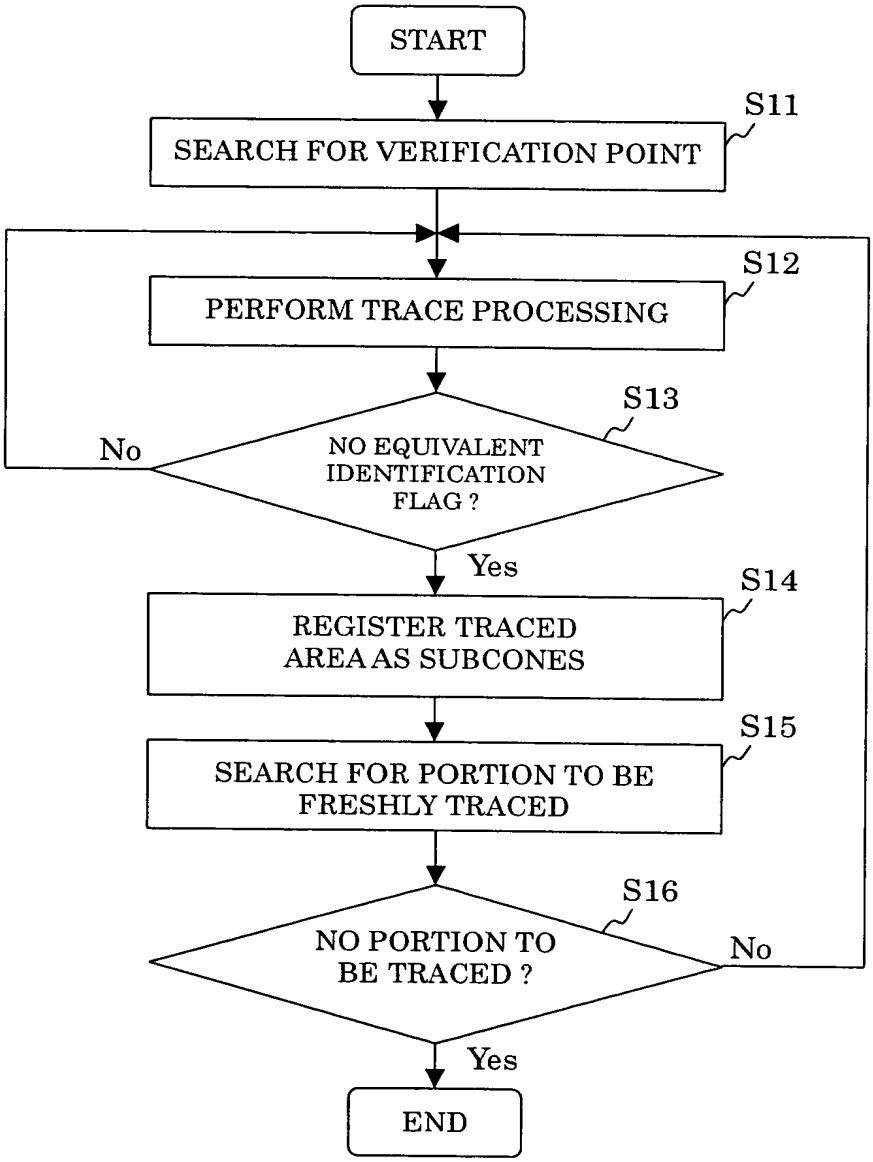

START
S11
SEARCH FOR VERIFICATION POINT
S12
PERFORM TRACE PROCESSING
S13
NO EQUIVALENT IDENTIFICATION FLAG ?
No
Yes
S14
REGISTER TRACED AREA AS SUBCONES
S15
SEARCH FOR PORTION TO BE FRESHLY TRACED
S16
NO PORTION TO BE TRACED ?
No
Yes
END

FIG.6A

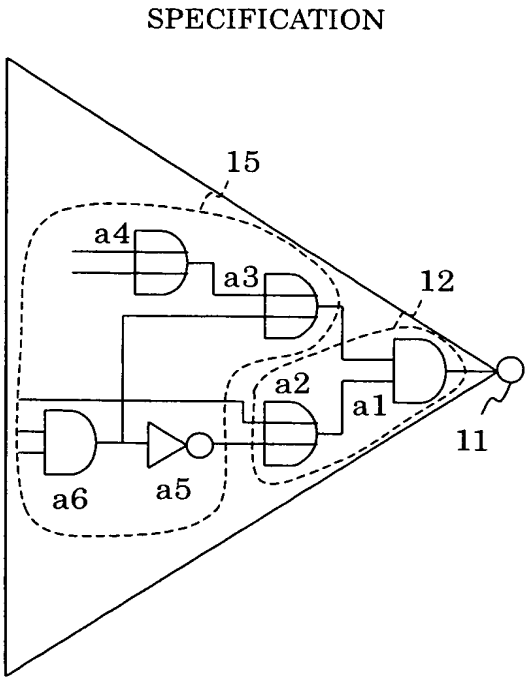


FIG.6B

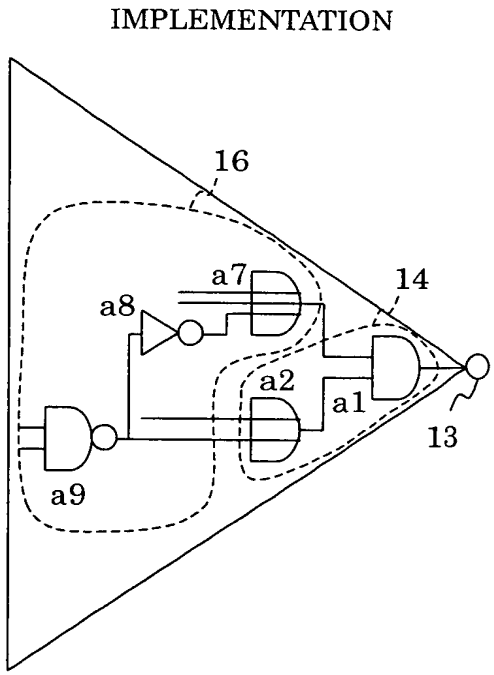


FIG.7A

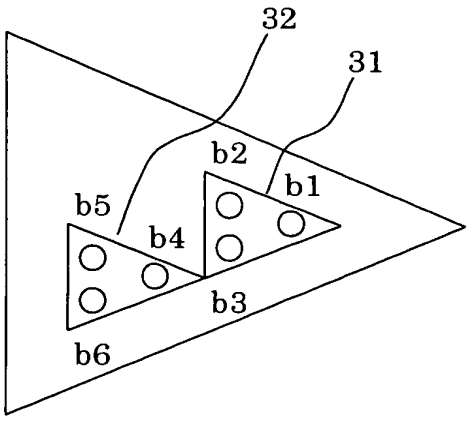


FIG.7B

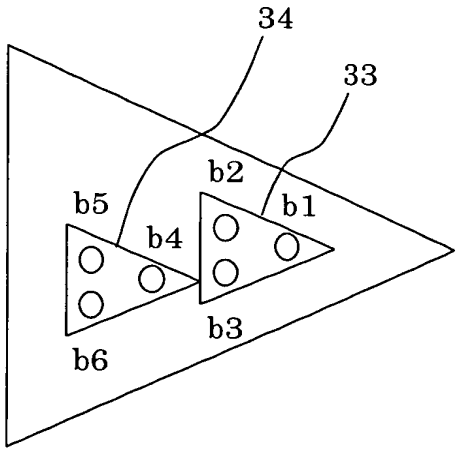


FIG.8

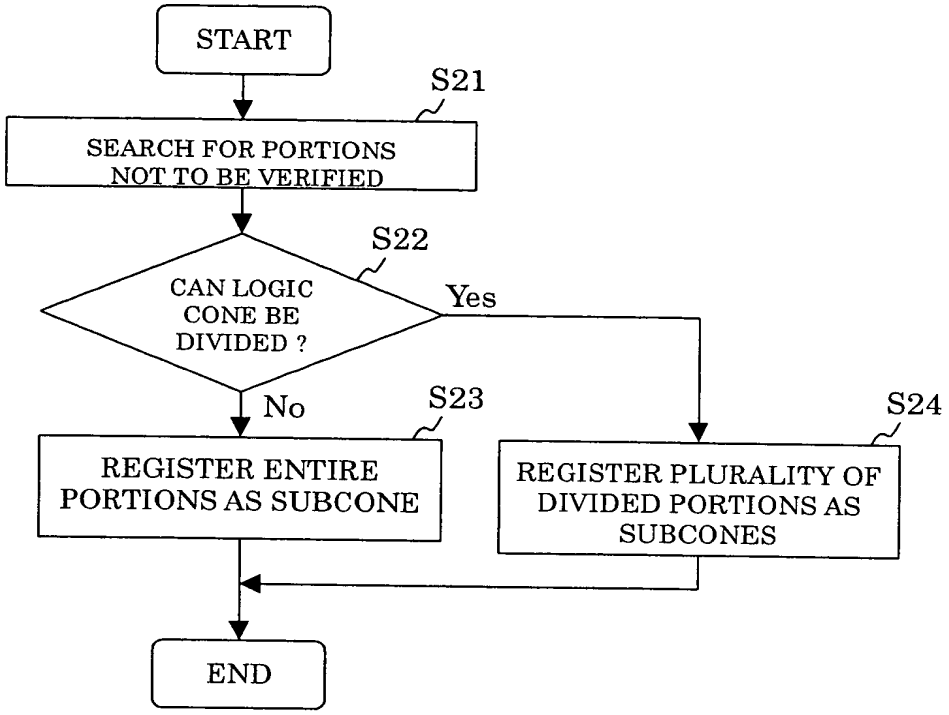


FIG.9A

FIG.9B

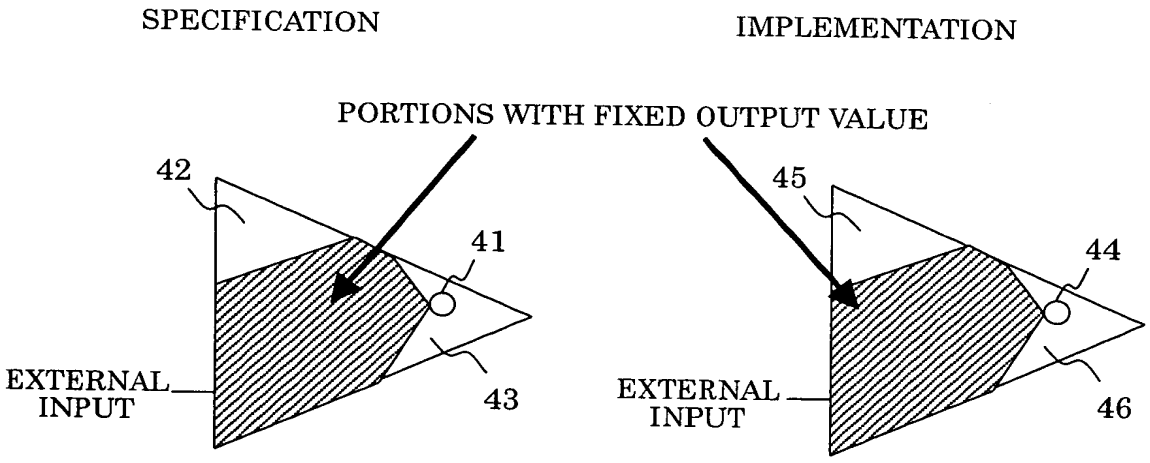


FIG. 10

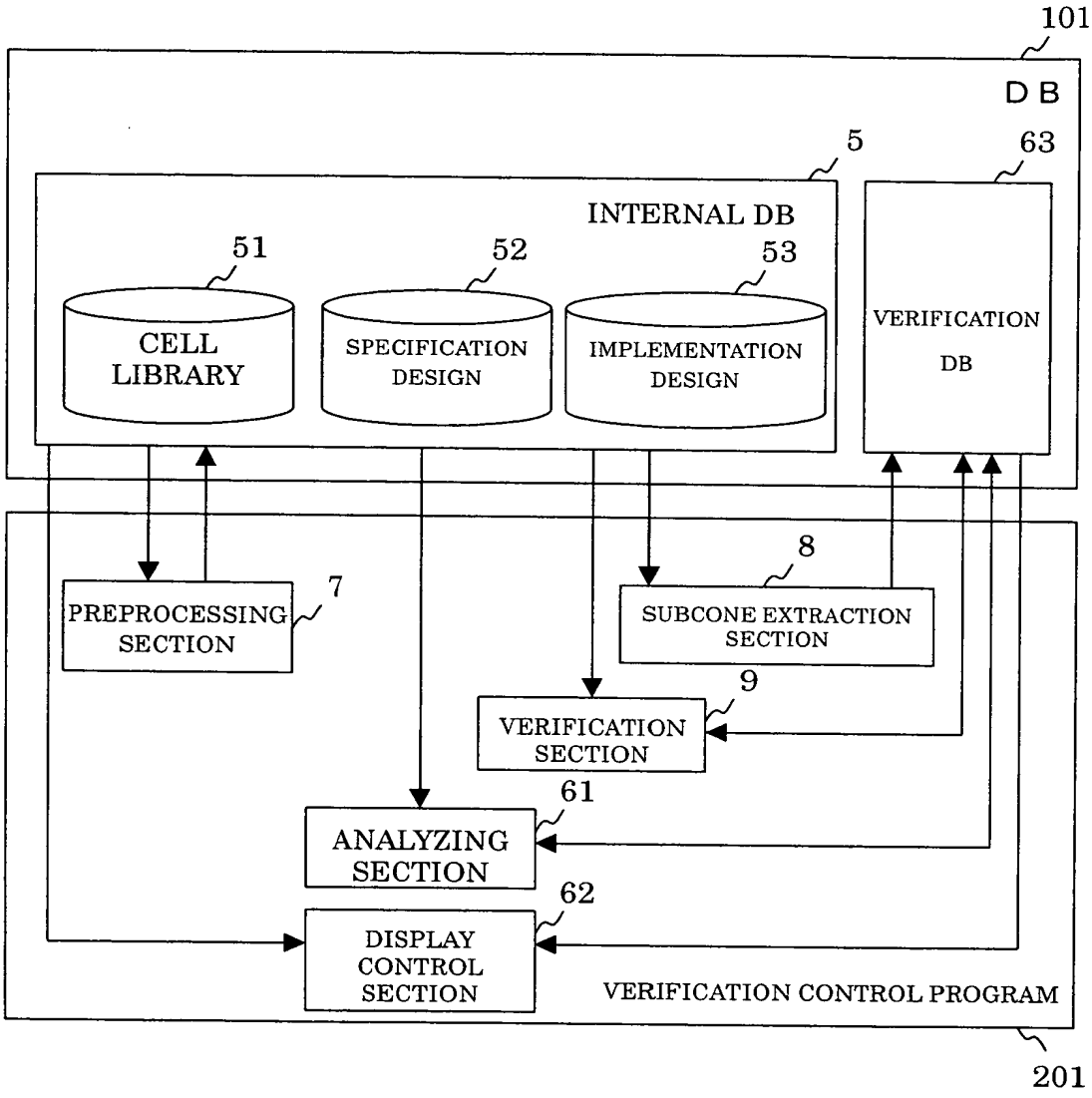

101
DB
5
63
INTERNAL DB
51
52
53
CELL LIBRARY
SPECIFICATION DESIGN
IMPLEMENTATION DESIGN
VERIFICATION DB
8
PREPROCESSING SECTION
7
SUBCONE EXTRACTION SECTION
9
VERIFICATION SECTION
61
ANALYZING SECTION
62
DISPLAY CONTROL SECTION
VERIFICATION CONTROL PROGRAM
201

FIG.11

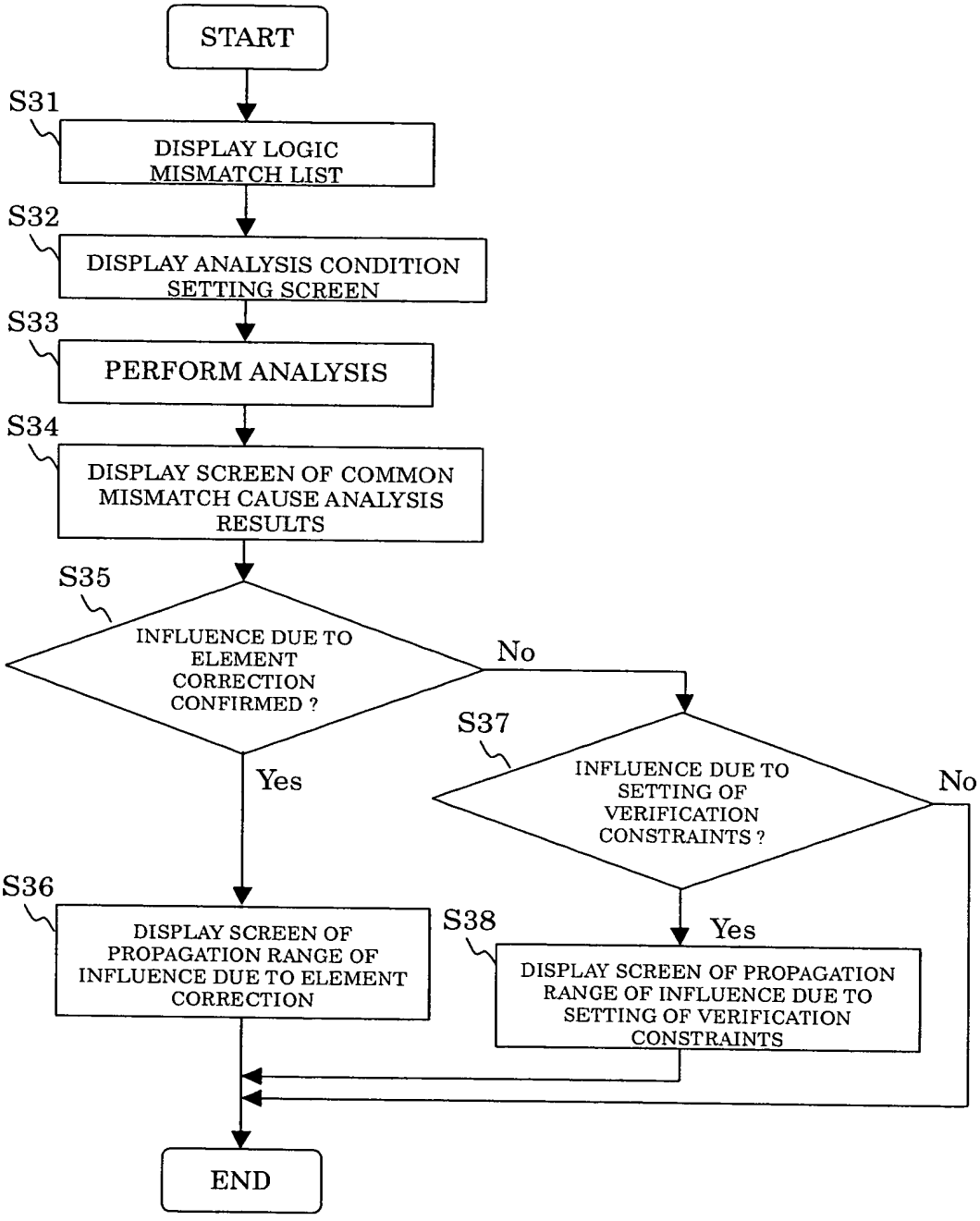

START
S31
DISPLAY LOGIC MISMATCH LIST
S32
DISPLAY ANALYSIS CONDITION SETTING SCREEN
S33
PERFORM ANALYSIS
S34
DISPLAY SCREEN OF COMMON MISMATCH CAUSE ANALYSIS RESULTS
S35
INFLUENCE DUE TO ELEMENT CORRECTION CONFIRMED ?
No
Yes
S37
INFLUENCE DUE TO SETTING OF VERIFICATION CONSTRAINTS ?
No
Yes
S36
DISPLAY SCREEN OF PROPAGATION RANGE OF INFLUENCE DUE TO ELEMENT CORRECTION
S38
DISPLAY SCREEN OF PROPAGATION RANGE OF INFLUENCE DUE TO SETTING OF VERIFICATION CONSTRAINTS
END

FIG.12

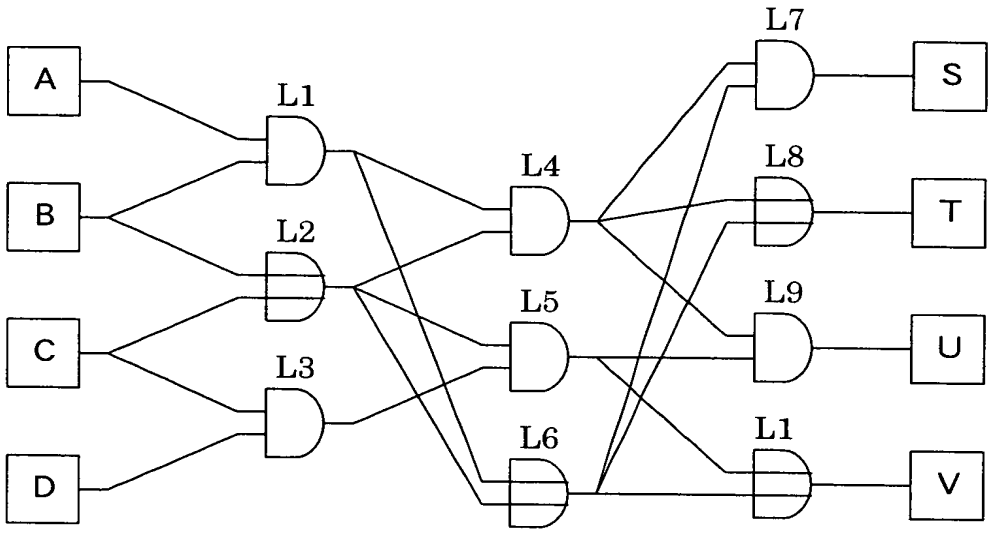

A
B
C
D
L1
L2
L3
L4
L5
L6
L7
L8
L9
L1
S
T
U
V

FIG.13

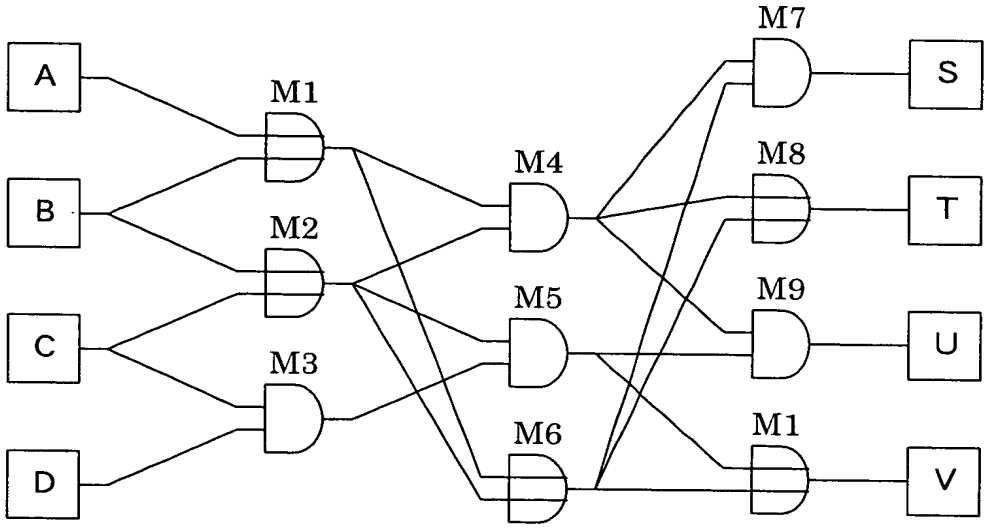

A
B
C
D
M1
M2
M3
M4
M5
M6
M7
M8
M9
M1
S
T
U
V

FIG. 14

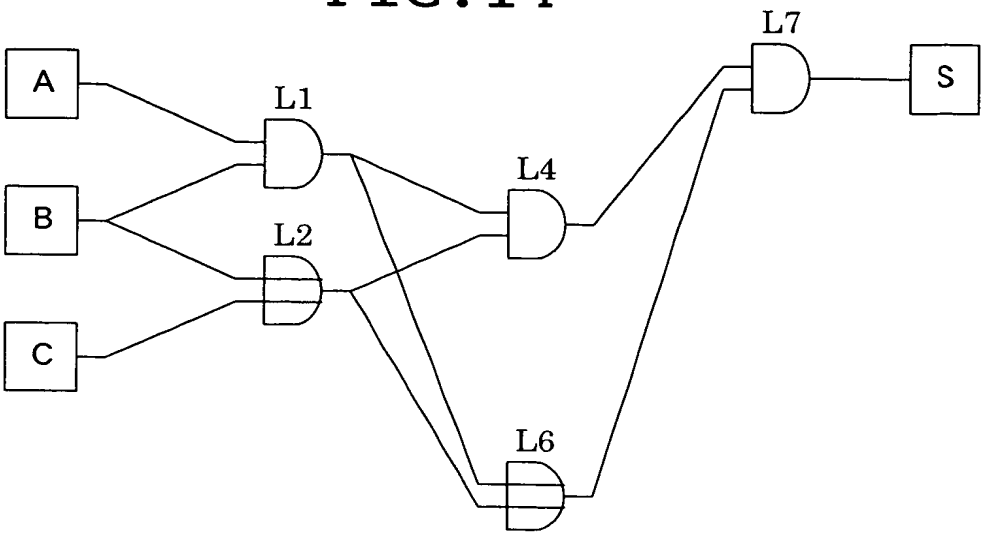

A
B
C
L1
L2
L4
L6
L7
S

FIG. 15

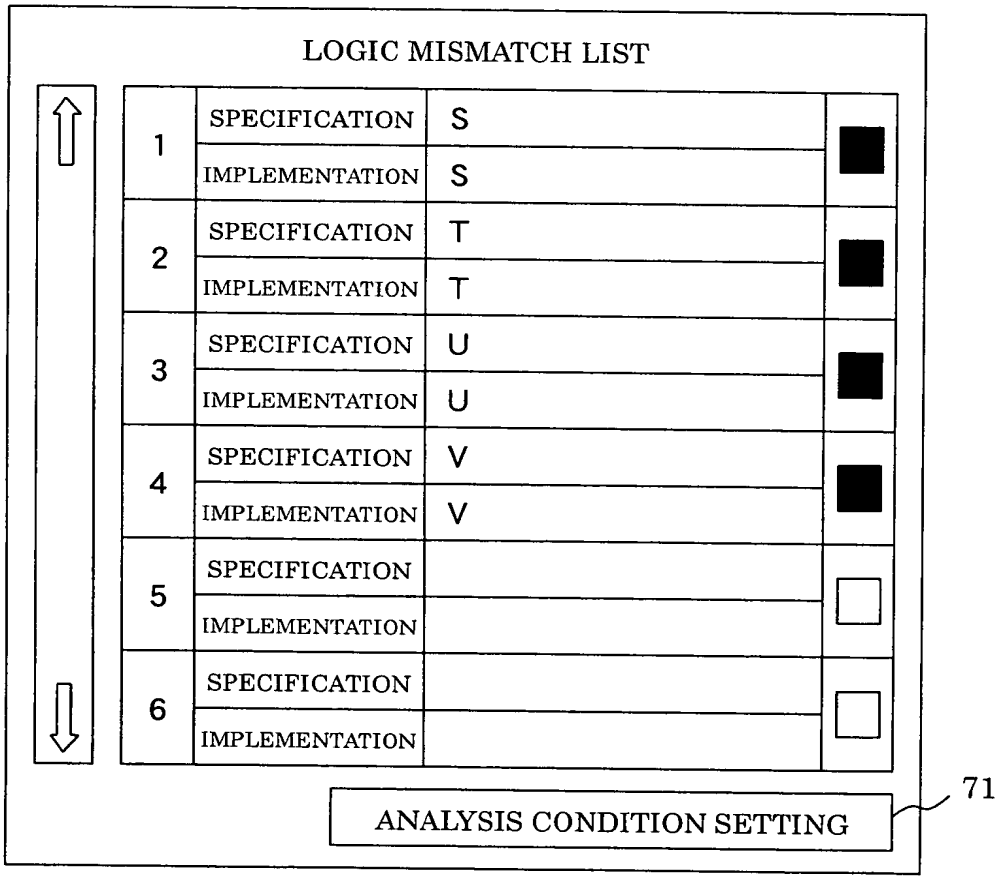

LOGIC MISMATCH LIST
1
SPECIFICATION
S
IMPLEMENTATION
S
2
SPECIFICATION
T
IMPLEMENTATION
T
3
SPECIFICATION
U
IMPLEMENTATION
U
4
SPECIFICATION
V
IMPLEMENTATION
V
5
SPECIFICATION
IMPLEMENTATION
6
SPECIFICATION
IMPLEMENTATION
ANALYSIS CONDITION SETTING
71

FIG.16

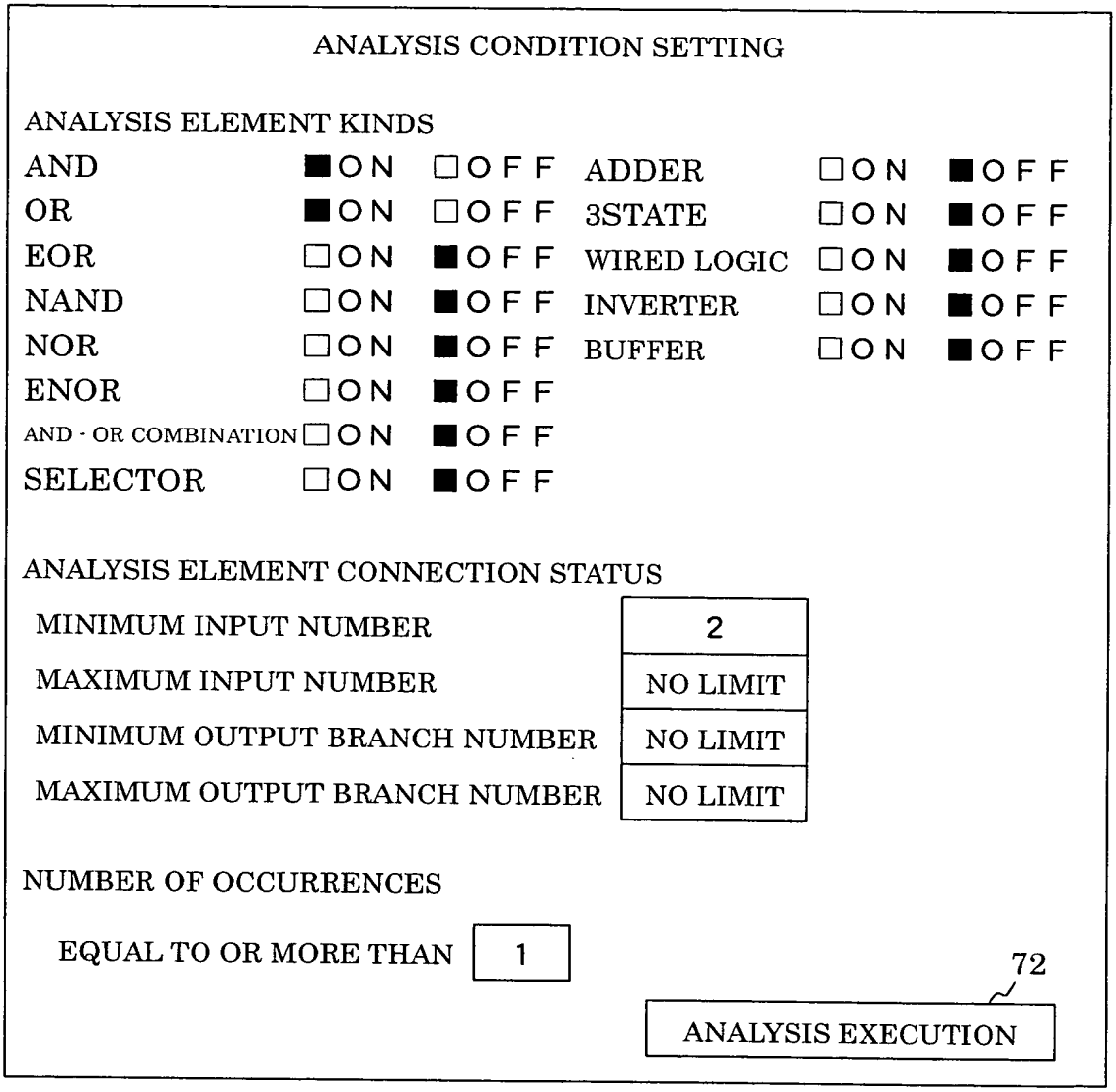

ANALYSIS CONDITION SETTING
ANALYSIS ELEMENT KINDS
AND ■ON □OFF
OR ■ON □OFF
EOR □ON ■OFF
NAND □ON ■OFF
NOR □ON ■OFF
ENOR □ON ■OFF
AND - OR COMBINATION □ON ■OFF
SELECTOR □ON ■OFF
ADDER □ON ■OFF
3STATE □ON ■OFF
WIRED LOGIC □ON ■OFF
INVERTER □ON ■OFF
BUFFER □ON ■OFF
ANALYSIS ELEMENT CONNECTION STATUS
MINIMUM INPUT NUMBER 2
MAXIMUM INPUT NUMBER NO LIMIT
MINIMUM OUTPUT BRANCH NUMBER NO LIMIT
MAXIMUM OUTPUT BRANCH NUMBER NO LIMIT
NUMBER OF OCCURRENCES
EQUAL TO OR MORE THAN 1
72
ANALYSIS EXECUTION

FIG. 17

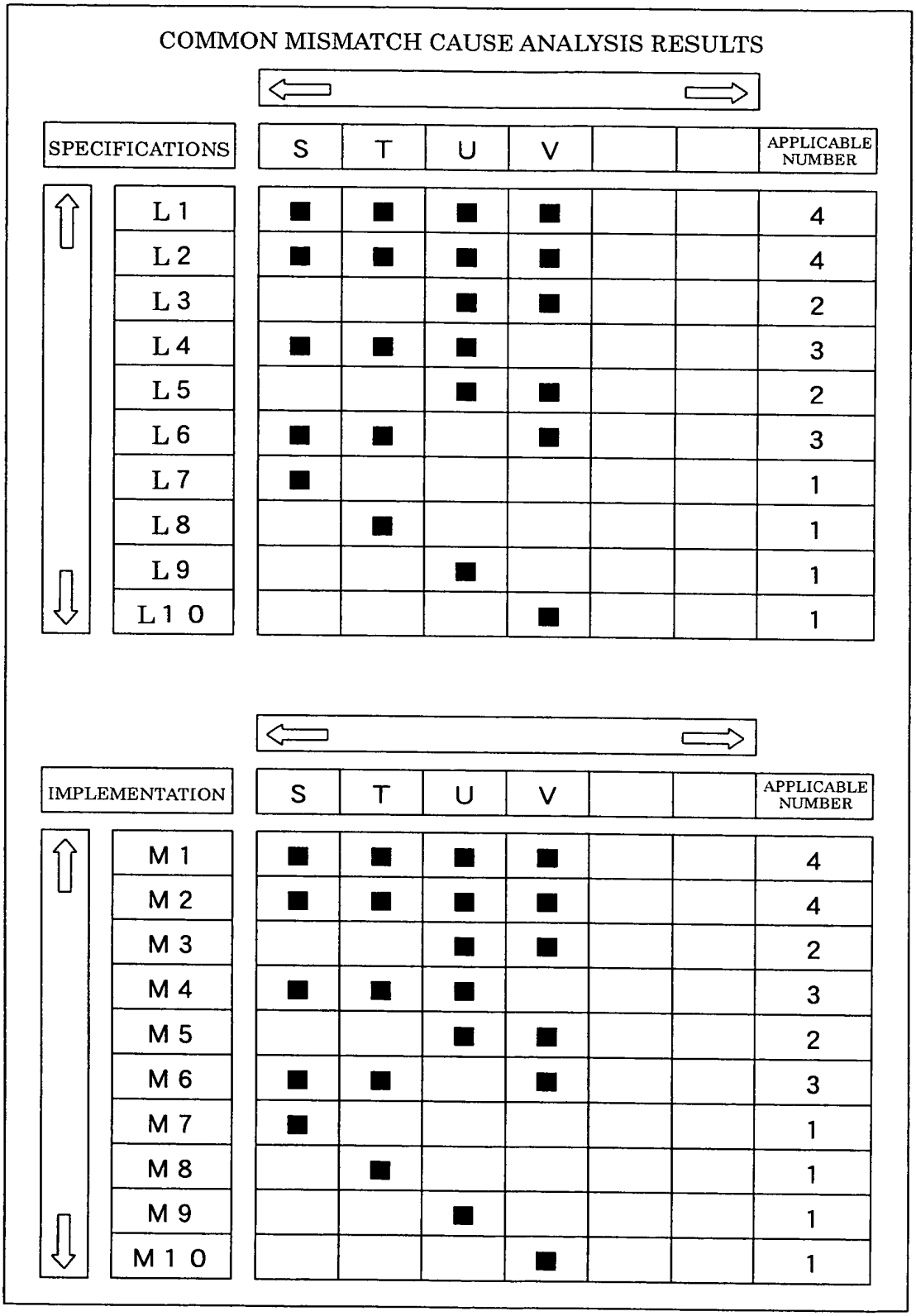

COMMON MISMATCH CAUSE ANALYSIS RESULTS
SPECIFICATIONS
S
T
U
V
APPLICABLE NUMBER
L1 4
L2 4
L3 2
L4 3
L5 2
L6 3
L7 1
L8 1
L9 1
L10 1
IMPLEMENTATION
S
T
U
V
APPLICABLE NUMBER
M1 4
M2 4
M3 2
M4 3
M5 2
M6 3
M7 1
M8 1
M9 1
M10 1

FIG.18

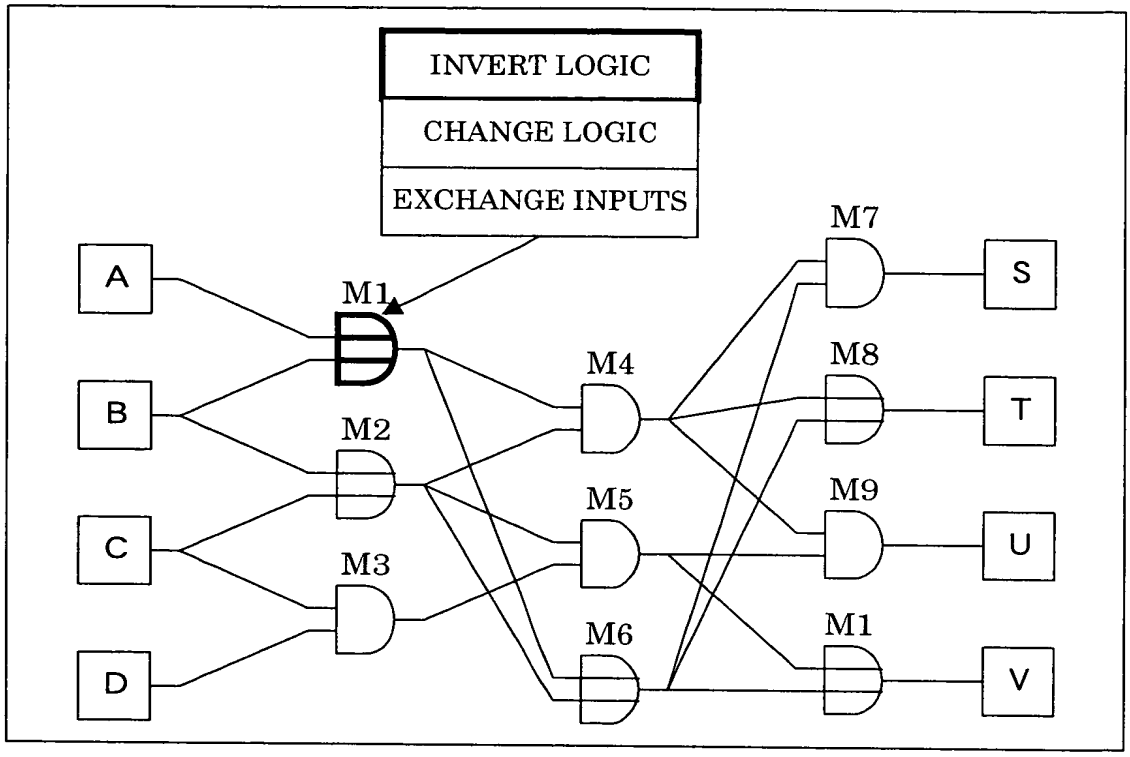

INVERT LOGIC
CHANGE LOGIC
EXCHANGE INPUTS
A
B
C
D
M1
M2
M3
M4
M5
M6
M7
M8
M9
M1
S
T
U
V

FIG.19

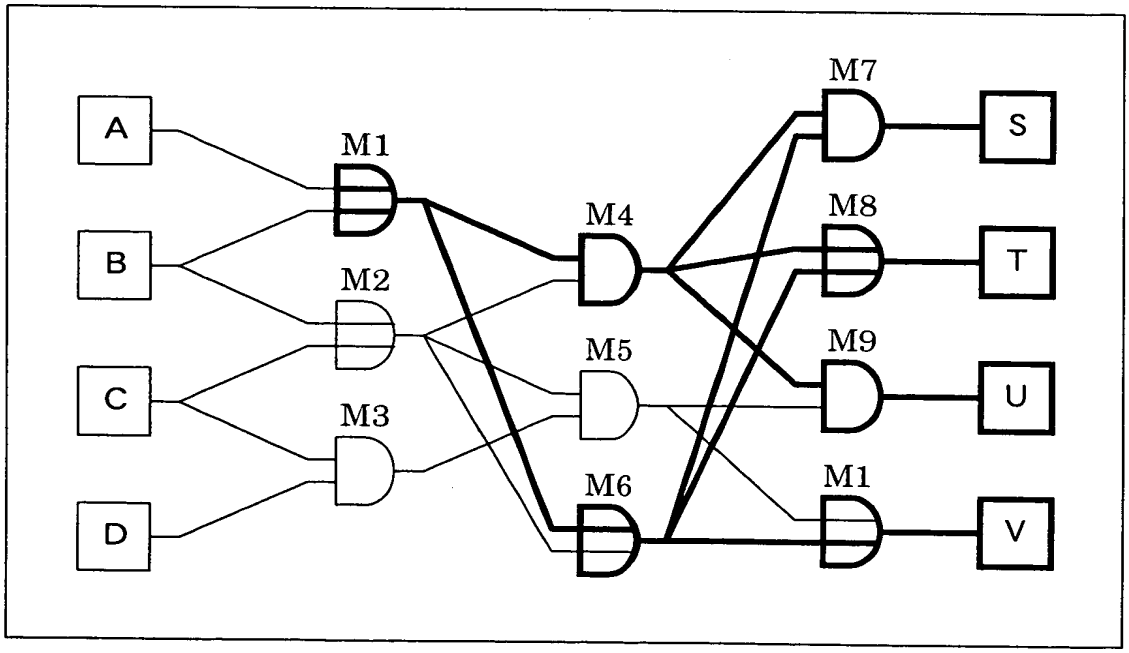

A
B
C
D
M1
M2
M3
M4
M5
M6
M7
M8
M9
M1
S
T
U
V

FIG.20

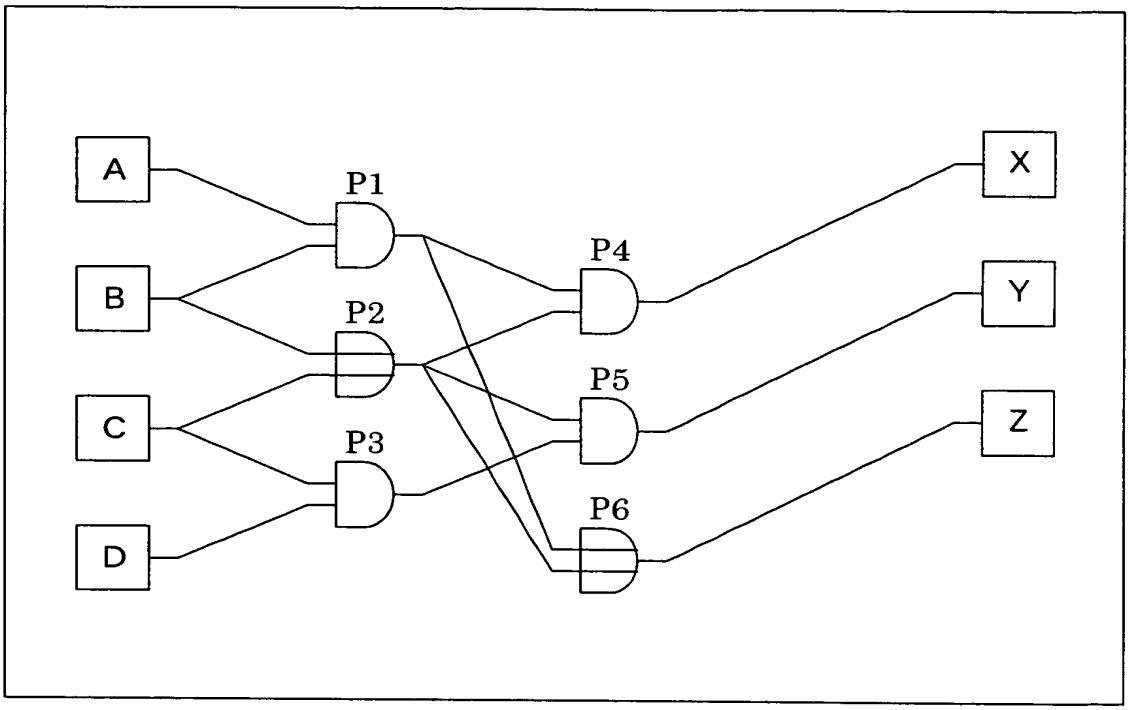


FIG.21

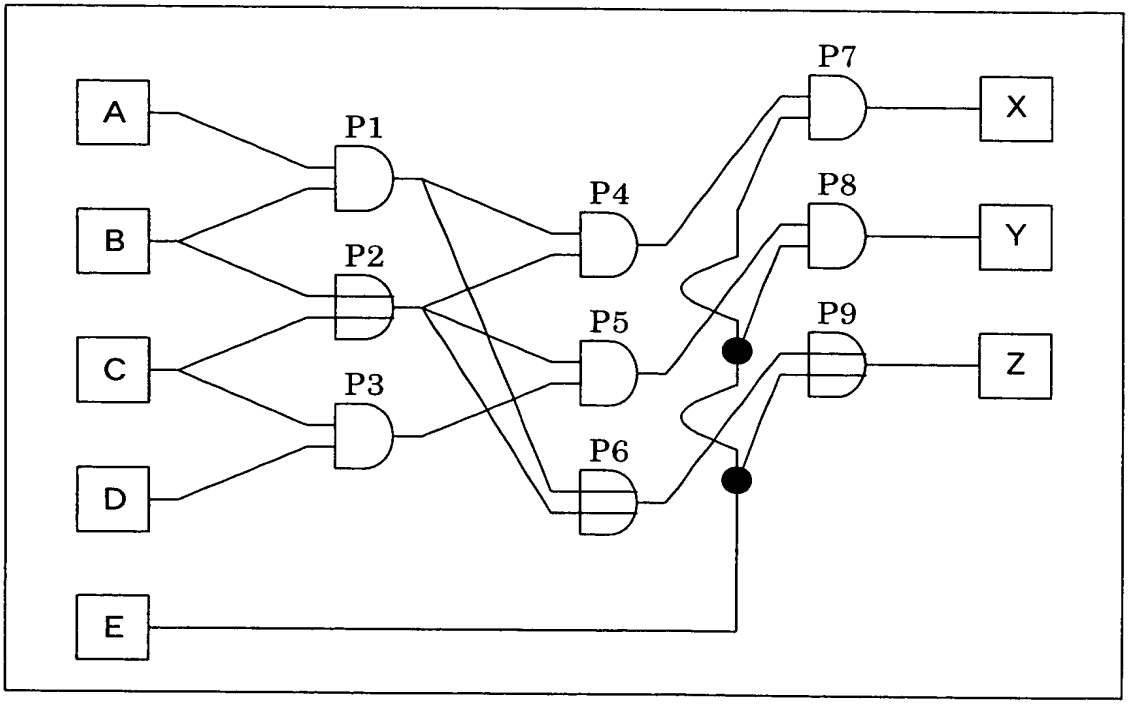


FIG. 22

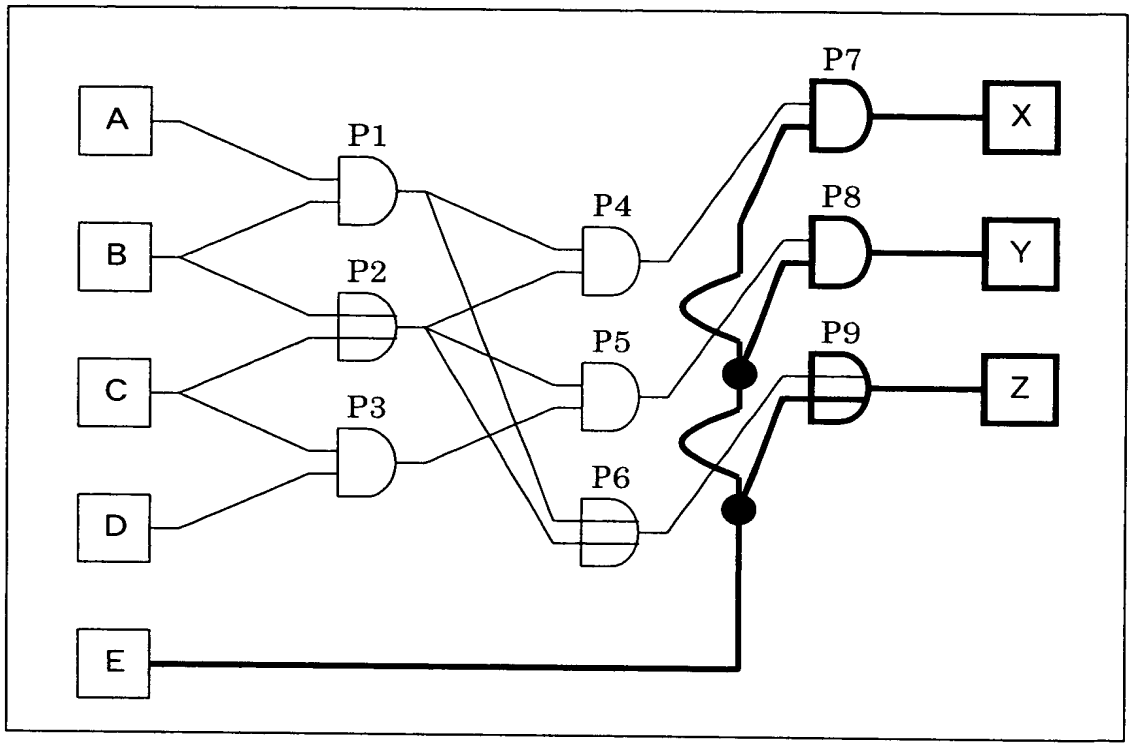
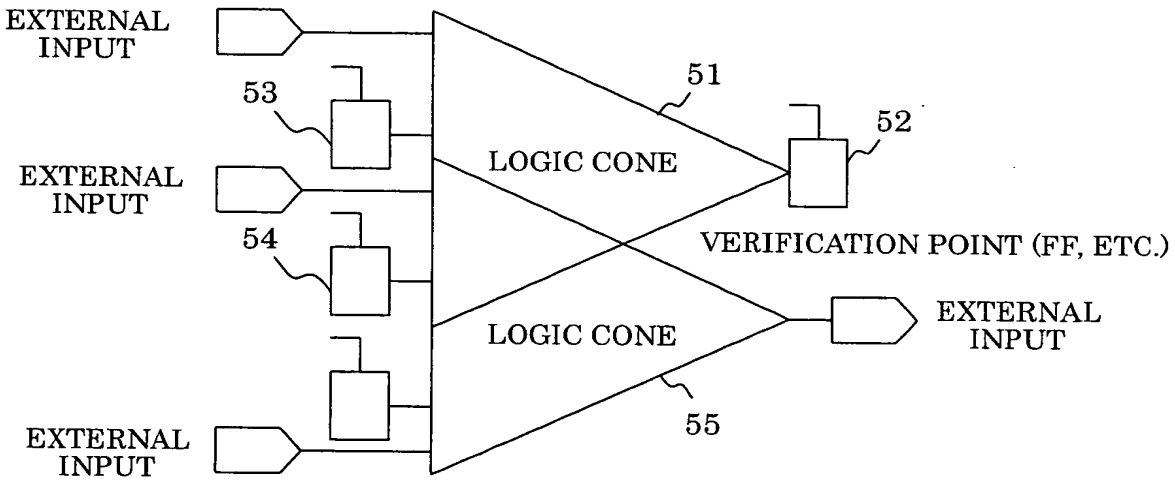

A
B
C
D
E
P1
P2
P3
P4
P5
P6
P7
P8
P9
X
Y
Z

FIG. 23


EXTERNAL INPUT
EXTERNAL INPUT
EXTERNAL INPUT
53
54
LOGIC CONE
LOGIC CONE
51
52
55
VERIFICATION POINT (FF, ETC.)
EXTERNAL INPUT